Amendments To The Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-13 Canceled.

Claim 14 (currently amended) A semiconductor device, comprising:

a substrate;

active areas formed within the substrate comprising a source area and a drain area;

a gate disposed between the source area and the drain area and insulated from the substrate by an oxide layer;

a first non-planar metallization level formed on the substrate in contact with the active areas including a first portion connected to the source area, a second portion connected to the drain area and a third portion at least partially covering the gate, the third portion including a portion covering a side face of the gate facing the source area, a portion covering a surface of the gate facing away form the substrate, and a portion covering a part of a side face of the gate facing the drain area, the portion covering the side face of the gate facing the drain area terminating at an end displaced from the substrate by a predetermined displacement; and

a second planar metallization level arranged spaced apart from the first metallization level above the substrate and connected to the second portion of the first metallization level via a through connection.

Claim 15 (previously presented) The semiconductor device of claim 14, wherein the first portion and the third portion of the first non-planar metallization level are connected.

Claim 16 (previously presented) The semiconductor device of claim 14, wherein between the first non-planar metallization level and the second planar metallization level an insulating layer is arranged, wherein in the insulating layer at least one through connection for a connection of the first non-planar metallization level to the second planar metallization level is formed.

Claim 17. (previously presented) The semiconductor device of claim 15, wherein the third portion implemented to shield the gate against electrostatic or electrodynamic interferences.

Claim 18 (previously presented) The semiconductor device of claim 15, wherein the predetermined displacement is set to be between about 250 nm and about 500 nm.

Claim 19. (previously presented) The semiconductor device of claim 18, and further comprising an oxide layer disposed between the third portion and the gate.

Claim 20. (previously presented) The semiconductor device of claim 19, and further comprising a reduced surface field area formed in the substrate and disposed between the gate and the drain area.

Claim 21. (previously presented) The semiconductor device of claim 14, wherein the predetermined displacement is set to be less than the thickness of the gate.